W6NBC PCB Trap (QST May 2018) notes N6MW 4/26/2018

John provided me a sample board to allow some measurements to be made with my hope of clarifying how the trap functions.

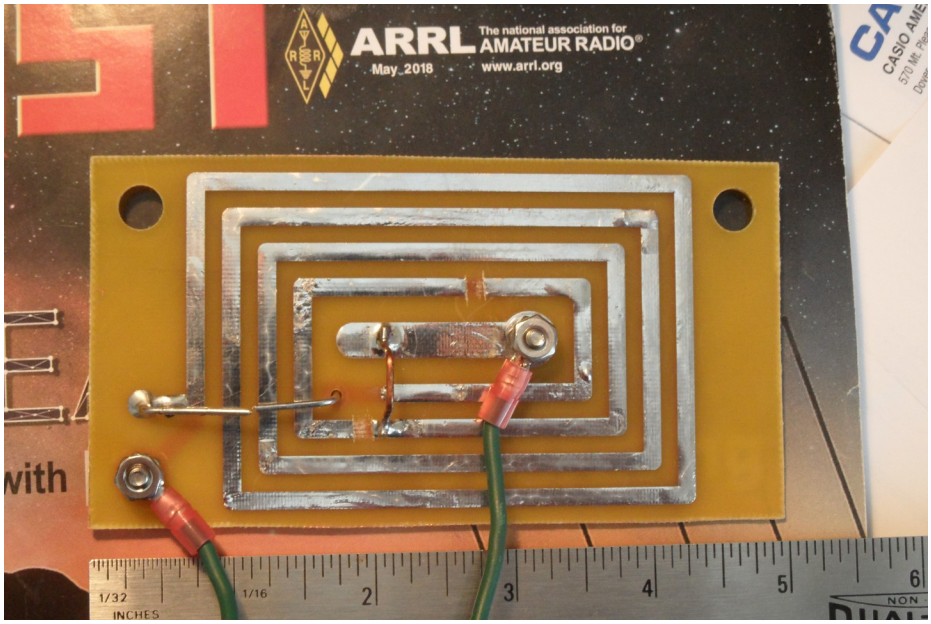

Figure 1. Board (after JP1 cut).

This particular board appears to be part of a cut-and-try experiment to determine tuning. It is a 5"X2.5" epoxy glass PCB etched accord to the article with the the JP1 plus a JP2 jumper with an experimental cut gap in the foil.

With the JP1connected his trap apparently has the conventional elements of a LC trap with the L provided by the connected back/front coil traces and the C provided by the same traces paired on opposite sides of the board.

First an estimate of the inductance. With JP1 connected, to make the inductance from the combined coils and the front and back of the board, this gives a combined ~ 7 turns with an average diameter of ~ 1.5". A standard coil inductance calculation then gives L ~ 3.5 microH.

The capacitance used differs from simply adding a parallel C since the jumper JP1 in addition to providing the L connection also has the effect of connecting the start of the trace on one side of the board to the end of the trace on the other side. This then effectively provides a short across the capacitor, at least at DC. It is not immediately apparent how this will impact the effective value of C at HF but it certainly must act to reduce C relative to that for a pair of strips positioned across a dielectric board.

For the capacitance, I estimate the back-to-back foil strips across the board to have a length (each side) of ~ 90 cm and a width of ~ 3.5 mm. Using a board thickness of 1.5 mm and dielectric constant of ~4, a standard calculation suggests C ~ 70 pfd for square plates but with an increase to ~ 140 pfd when the extensive edge effects are accounted for. The correction might be more than that since the loops are fairly closely spaced. Note that this estimate assumes JP1 is NOT connected.

Measurements of magnitude of impedance, |Z|, with frequency were taken by an MFJ-259B poor man's network analyzer so *caveat emptor*. This was done using shortish leads connected to the two sides of the trap and with JP1 connected. The MFJ measurements were taken from 5 to 34 MHz with the restriction that |Z| can be no more that about 600 ohms. The six data points were then fit with commercial software assuming a parallel LC circuit and the results are shown in the figure. In principle one could include some resistance as well but it was found only that any parallel R would have to be quite large so it is ignored.

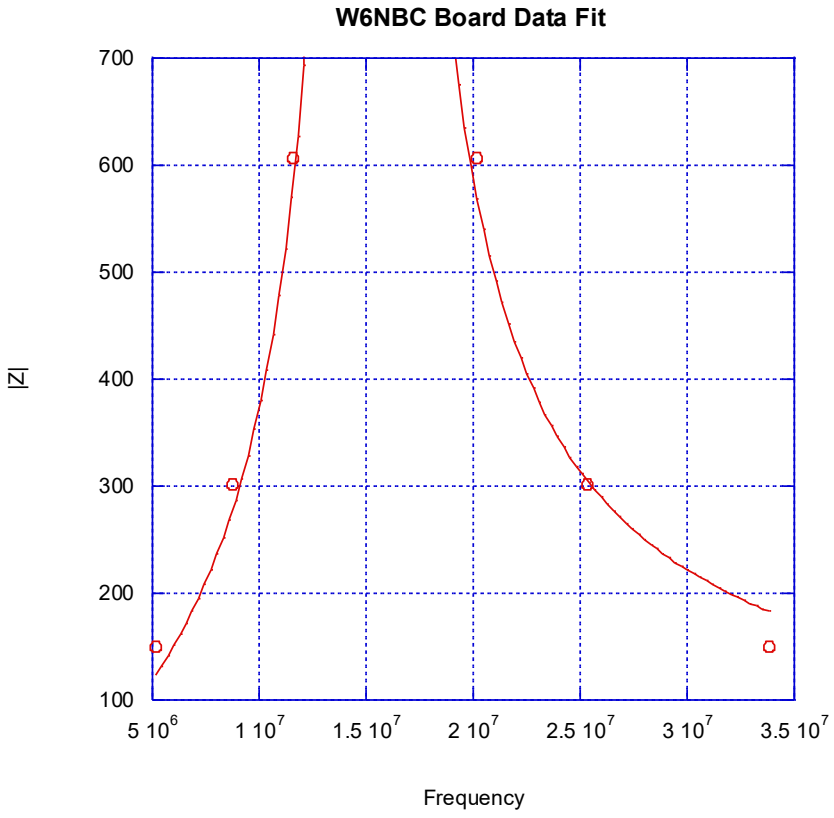

Figure 2. Plot of measured |Z| and fit.

The data fit, assuming a parallel LC circuit, provided L ~ 3.4 microH and C ~ 32 pfd both with uncertainties of ~ 10%.

For the L this is close to the estimate above but keep in mind that the parameters for the estimate are rather loose. In any case, it certainly seems as if L is reasonably described by the connected coils on the two sides of the board.

As for C, the fit value is substantially lower than the rough estimate for the case of JP1 NOT connected, as anticipated before.

As the final step, the jumper JP1 was cut and |Z| again measured over a similar frequency range as before. As a sidelight, the |Z| looks rather like a series LC circuit, which may not be meaningful, but at

low frequencies, where C dominates, the value of C can be estimated as C(no JP1) ~ 85 pfd. This value is in the range that was estimated above. And as expected, it is distinctly higher than the result fit for a parallel LC circuit before of 32 pfd with JP1 connected.

So it appears that the C which results from this PCB trap connection takes a substantal hit from that which might have been expected as a result of the need to provide the JP1 to form the L due to the resulting (indirect) short circuit which cannot be avoided with this design.

An alternative design that might reduce the need for cut-and-try would be to have the some coils as currently used for L but provide C in a more conventional way with rectangular patchs in the center of the PCB. Of course the back-to-back traces will still provide some additional hard to determine C but that effect could be reduced with narrower traces and/or offsetting the traces on front and back. Still the back-to-back traces for C is a part of the (perhaps deceptive) charm of the existing design.